CLAIMS

What is claimed is:

1. A data transfer system comprising:

a plurality of peripheral interfaces;

a first memory; and

a programmable direct memory access module coupling the first memory to each of the plurality of peripheral interfaces, wherein the programmable direct memory access module configures selectively programmable direct memory access data channels between the first memory and respective ones of the plurality of peripheral ~~interfaces.~~

2. The data transfer system of Claim 1 further comprising a first processor coupled to the programmable direct memory access module and associated with the first memory.

3. The data transfer system of Claim 1 further comprising a second memory coupled to the programmable direct memory access module, wherein the programmable direct memory access module configures the selectively programmable direct memory access data channels between the second memory and respective ones of the plurality of peripheral interfaces.

4. The data transfer system of Claim 3 further comprising a second processor coupled to the programmable direct memory access module and associated with the second memory.

5. The data transfer system of Claim 3 wherein the selectively programmable direct memory access data channels are configured between the first memory and the second memory.

6. The data transfer system of Claim 1 wherein the programmable direct memory access module includes a programmable processor.

7. The data transfer system of Claim 6 wherein the programmable direct memory access module further includes a direct memory access controller coupled to the programmable processor, wherein the programmable processor configures the selectively programmable direct memory access data channels between the first memory and respective ones of the plurality of peripheral interfaces via a dedicated direct memory access data transfer channel of the direct memory access controller.

8. The data transfer system of Claim 1 wherein the programmable direct memory access module further comprises a programmable scheduler for prioritizing data transfers over respective ones of the selectively programmable direct memory access data channels.

9. A direct memory access system comprising:

a direct memory access controller establishing a direct memory access data channel and including a first interface for coupling to a memory;

a second interface for coupling to a plurality of nodes; and

a processor coupled to the direct memory access controller and coupled to the second interface, wherein the processor configures the direct memory access data channel to transfer data between a programmably selectable respective one or more of the plurality of nodes and the memory.

10. The system of Claim 9 wherein the plurality of nodes are one of a plurality of peripheral interfaces and a memory interface.

11. The system of Claim 9 further comprising a programmable scheduler coupled to the processor for prioritizing the data transfer via the direct memory access data channel such that the data transfer occurs according to predetermined priorities.

12. A method for performing direct memory access, the method comprising:

receiving a request for a direct memory access data transfer;

configuring code to establish a direct memory access data transfer channel between a node specified by the request and a direct memory access interface; and

transferring data between the node and the direct memory access interface along the direct memory access data transfer channel.

13. The method of Claim 12 wherein the receiving step comprises receiving a timed request for a direct memory access data transfer.

14. The method of Claim 12 further comprising prioritizing the data to be transferred via the direct memory access data transfer channel.

15. The method of Claim 14 further comprising interrupting the transferring of data in the event a higher priority direct memory access data transfer is required.

16. The method of Claim 15 further comprising resuming the interrupted transfer of data upon completion of the higher priority direct memory access data transfer.

17. A memory access system comprising:

a memory;

a multiplexer coupled to the memory via a first bus having a first bus width;

a host processor coupled to the multiplexer via a second bus having a second bus width, wherein the second bus width is less than the first bus width; and

a display controller coupled to the multiplexer via a third bus having a third bus width the same as the first bus width to allow the memory to be utilized as a buffer for both the host processor and the display controller such that one of the display controller and the host processor may access the memory without restricting the ability of the other of the host processor or display controller to access the memory.

18. The memory access system of Claim 17 wherein the first bus width is 128 bits.

19. The memory access system of Claim 17 wherein the second bus width is a predetermined number of bits, the predetermined bit number being either 8, 16, or 32 bits.

20. The memory access system of Claim 17 further comprising a programmable direct memory access module coupled to the multiplexer via a fourth bus having a fourth bus width less than the first bus width to allow the memory to be used as a direct memory access node.

21. The memory access system of Claim 20 wherein the fourth bus width is a predetermined number of bits, the predetermined bit number being either 8, 16, or 32 bits.

22. The memory access system of Claim 17 wherein the memory is embedded onto a processor platform including the host processor and the display controller.

23. A method of memory refresh, the method comprising:

providing a dynamic random access memory having a predetermined capacity; and

periodically refreshing a portion of the dynamic random access memory less than its predetermined capacity to reduce power consumed as the memory portion is refreshed.

24. The method of Claim 23 further comprising adjusting a refresh rate of the dynamic random access memory based on ambient temperature, and memory is the periodically refreshed by periodically refreshing the portion at the adjusted refresh rate.

25. The method of Claim 23 wherein the memory capacity includes a predetermined total number of rows thereof and the memory portion comprises a number of rows of the dynamic random access memory less than its predetermined total number of rows.

26. A method of memory refresh, the method comprising:

providing a dynamic random access memory;

adjusting a refresh rate of the dynamic random access memory based on ambient temperature; and

periodically refreshing the dynamic random access memory at the adjusted refresh rate with refreshing occurring less frequently at lower ambient temperatures to reduce power consumed at lower temperatures.

27. The method of Claim 26 wherein the periodically refreshing step comprises periodically refreshing a portion of the dynamic random access memory less than its predetermined capacity of the memory to reduce power consumed as the memory portion is refreshed.

28. The method of Claim 26 wherein the memory capacity includes a predetermined total number of rows thereof and the memory portion comprises a number of rows of the dynamic random access memory less than its predetermined total number of rows.

29. A processor communication system, comprising:

a host processor direct memory access interface;

one or more peripheral ports;

a data bus for conveying data between said host processor direct memory access interface and said one or more peripheral ports; and

a programmable controller comprising a plurality of registers in communication with said data bus for maintaining data communication, with said programmable controller being operable for storing and retrieving data from the plurality of registers to establish multiple data transfers between said host processor direct memory access interface and said one or more peripheral ports.

30. A system as recited in claim 29, comprising a second processor direct memory access interface, wherein said programmable controller is operable for establishing multiple data transfers between said host processor direct memory access interface, said second processor direct memory access interface, and said one or more peripheral ports.

31. A system as recited in claim 30, wherein said programmable processor prioritizes the multiple data transfers established by storing and retrieving the data from the plurality of registers for data transfer between said host processor direct memory access interface, said second processor direct memory access interface, and said

one or more peripheral ports.

32. A system as recited in claim 30, wherein said second processor direct memory access interface comprises a digital signal processor direct memory access interface to random access memory associated with a digital signal processor.

33. A system as recited in claim 32, wherein said programmable controller is operable for establishing multiple virtual direct memory access channels between said host processor direct memory access interface, said digital signal processor, direct memory access interface, and said one or more peripheral ports.

34. A system as recited in claim 33, comprising embedded dynamic random access memory for use with the host processor.

35. A memory refresh system comprising:

a temperature sensor for providing a temperature measurement;

a memory coupled to the temperature sensor for providing a temperature dependent count value based upon the temperature measurement; and

a count register coupled to the memory for storing the temperature dependent count value used to determine a temperature dependent refresh cycle for a dynamic random access memory.

36. The system of Claim 35 further comprising:

a comparator coupled to the count register; and

a counter coupled to the comparator, wherein the comparator outputs a signal when the counter matches the temperature dependent count value within the count register.

37. The system of Claim 36 further comprising a refresh enable unit coupled to the comparator, wherein the refresh enable unit provides a refresh enable signal responsive to the signal output from the comparator, wherein providing the temperature dependent refresh cycle for the dynamic random access memory.